Lecture 5
Device Systems

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Introduction

- **Description of the internal devices and systems of the MSP430;**

- **It includes descriptions of the:**
  - Internal system reset;
  - Clock sources;
  - Interrupt management;
  - Low-power operating modes.

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System reset (1/5)

- **The MSP430 families make use of two independent reset signals:**
  - Hardware reset signal - POR (Power On Reset);
  - Software reset signal – PUC (Power Up Clear).

- **Different events determine which one of the reset signals is generated;**

- **Sources that can generate a POR:**
  - Initial device power up;
  - Low signal at the reset pin (RST/NMI) when this is configured in reset mode;
  - Low signal at the supervisory voltage system (SVS) when the register bit PORON is high.

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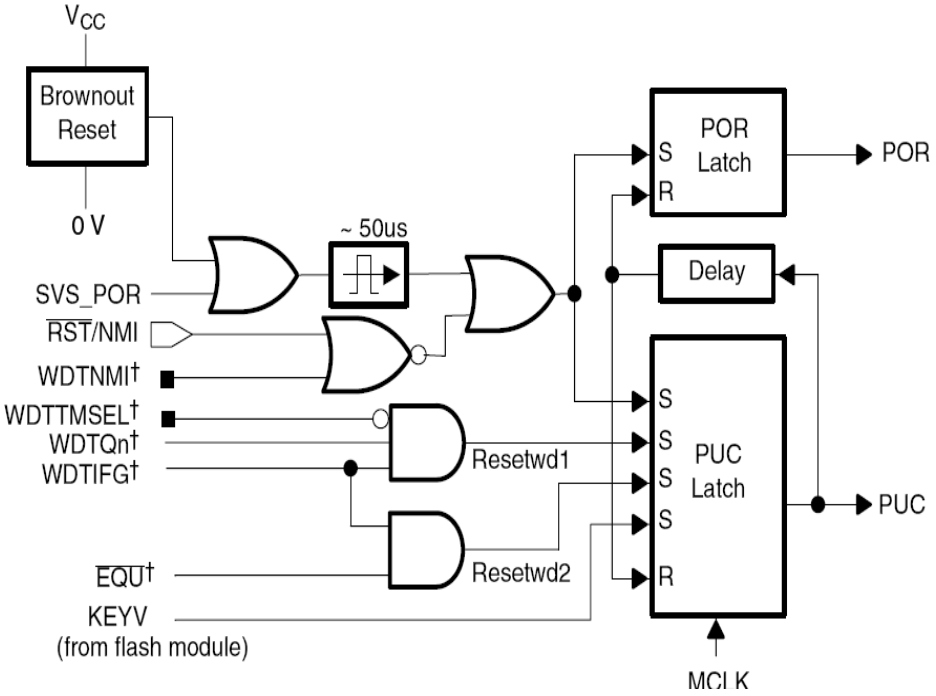
System reset (2/5)

- **Sources that can generate a PUC:**
  - Active POR signal;
  - Watchdog timer (WDT) expired when it is configured in supervision mode;
  - Flash memory access control registers security key violation.



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System reset (3/5)

❑ Conditions:

- Hardware reset signal (POR) is active then:
  - SR is reset;
  - PC is loaded with the address in location 0FFFEh;
  - Peripheral registers all enter their power up state.

- Software reset signal (PUC) is active then:
  - SR is reset;
  - PC is loaded with either the reset vector (0FFFEh), or the PUC source interrupt vector;
  - Only some peripheral registers are reset by PUC.

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System reset (4/5)

- **All 2xx and 4xx MSP430 devices possess a reset circuit**
  - By power source disturbance identified by Brown Out Reset (BOR);

- **This circuit is an enhanced POR system:**
  - Includes a hysteresis circuit;
  - Device stays in reset mode until voltage is higher than the upper threshold (VB_IT+):
    - BOR takes 2 msec to be inactive and allow the program execution by CPU;
  - When voltage falls below the lower threshold (VB_IT-):
    - BOR circuit will generate a reset signal;
    - Suspends processor operation until the voltage rises up above the lower threshold inferior value.

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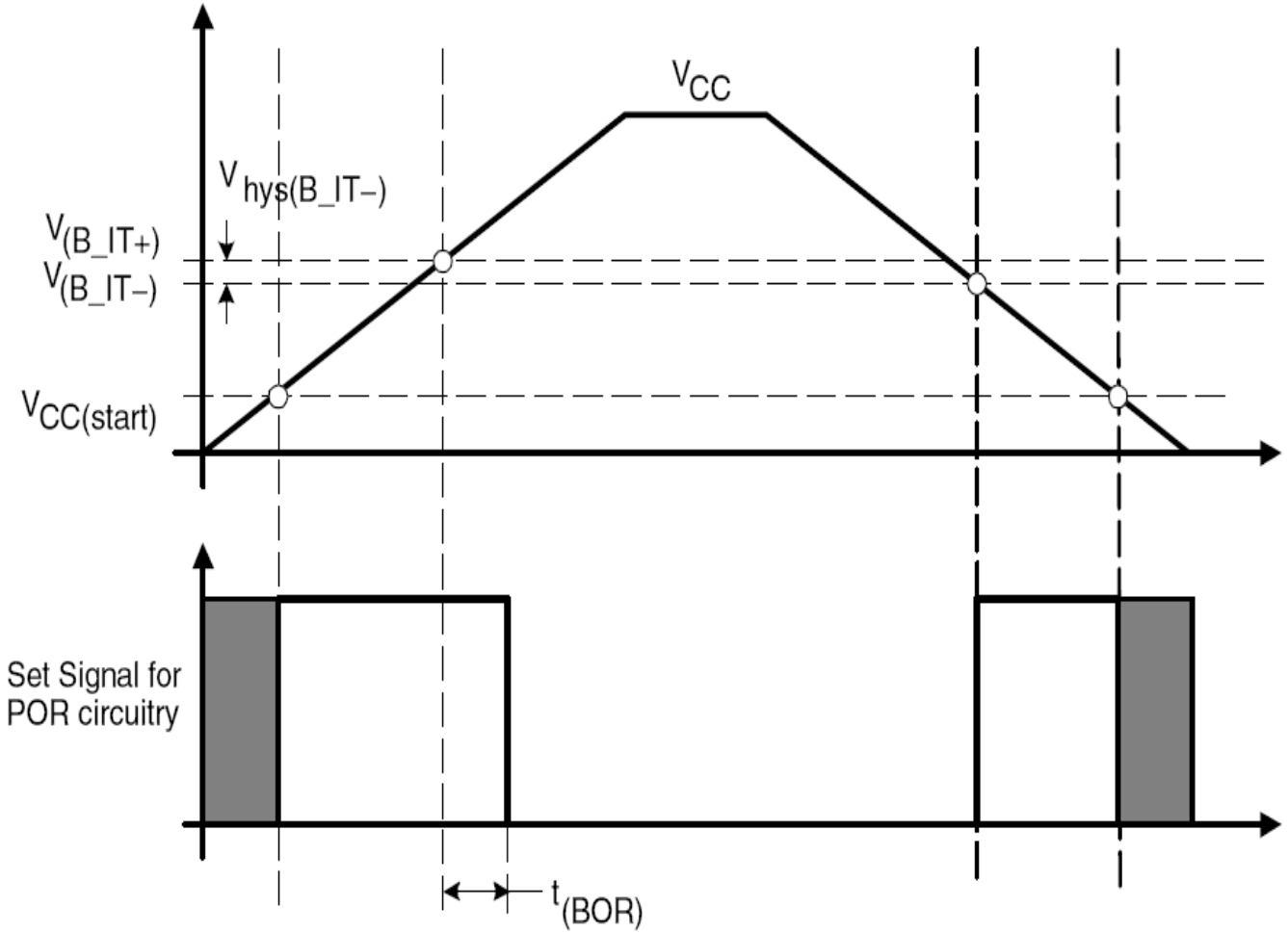
System reset (5/5)

- **Brownout timing:**



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System clocks (1/24)

- **Allows the CPU and peripherals to operate from different clock sources;**
- **The system clocks depend on the device in the MSP430 family:**
  - **MSP430x2xx:**
    - The Basic Clock Module+ (BCM+);
      - One or two oscillators (depending on the device);
      - Capable of working with external crystals or resonators;
      - Internal digitally controlled oscillator (DCO);
      - Working frequency to up 16 MHz;
      - Lower power consumption;
      - Lower internal oscillator start-up time.

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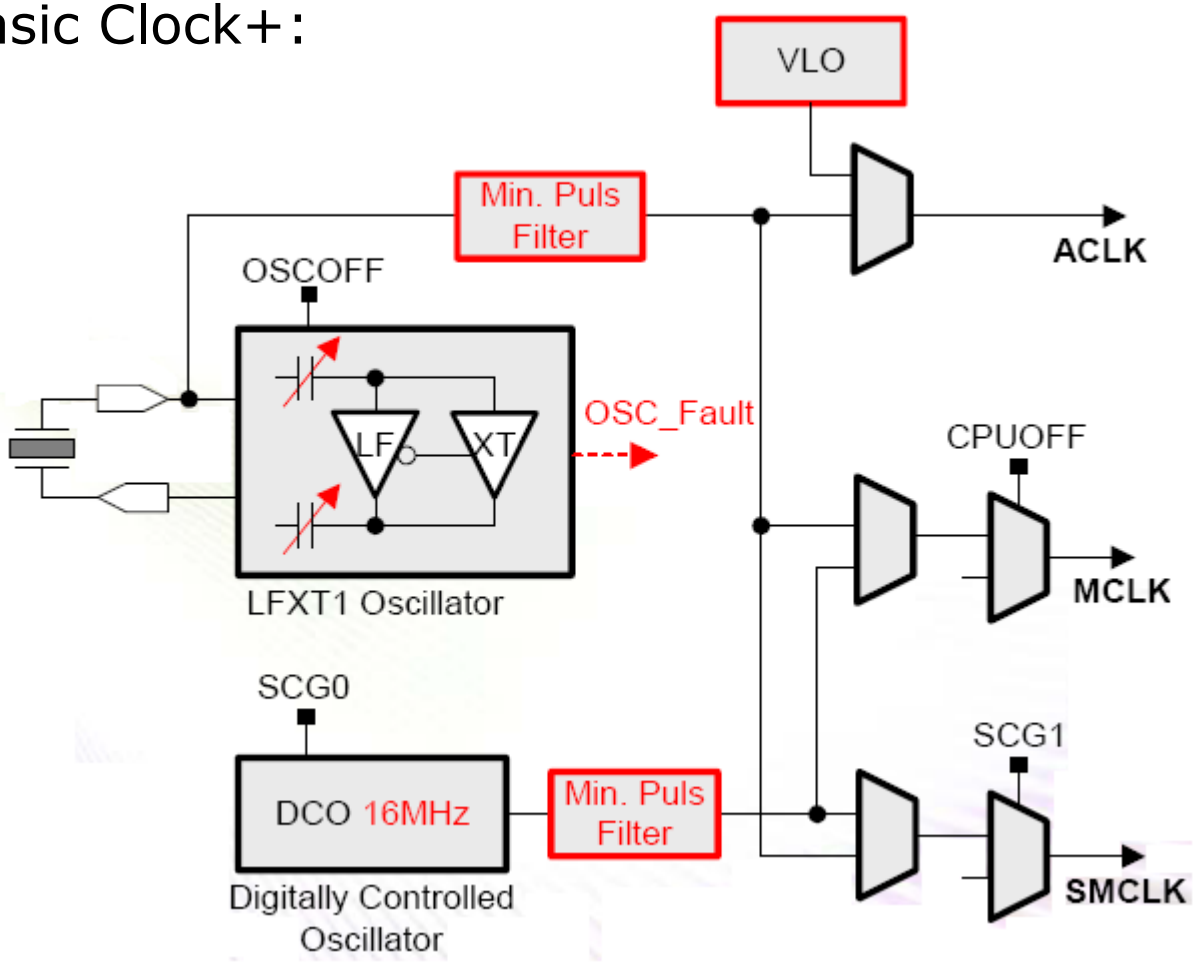
System clocks (2/24)

- **MSP430x2xx:**
  - Basic Clock+:



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System clocks (3/24)

- **MSP430x4xx:**
  - Frequency Locked Loop (FLL+):
    - One or two oscillators (depending on the device);
    - Capable of working with external crystals or resonators;
    - Internal digitally controlled oscillator (DCO), adjusted and controlled by hardware;
    - Synchronized to a high-frequency internal clock from a low frequency external oscillator.

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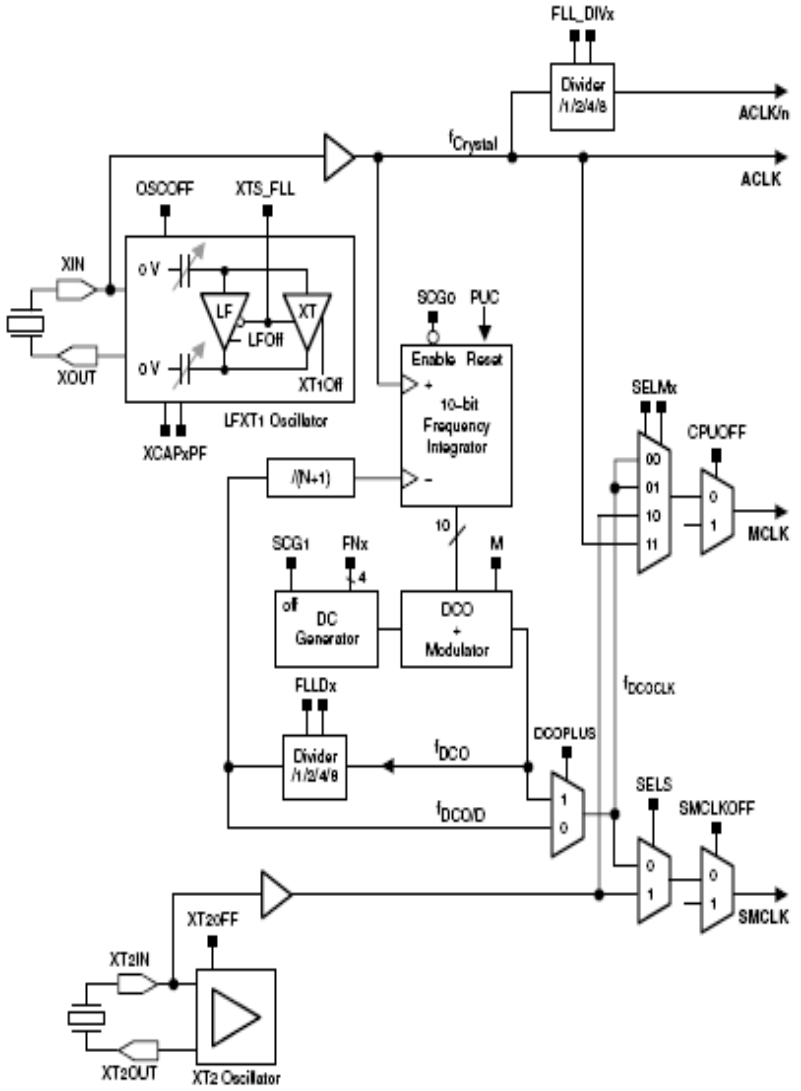
System clocks (4/24)

- **MSP430x4xx:**
  - FLL+:



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System clocks (5/24)

- **The clock sources from these oscillators can be selected to generate different clock signals:**
  - **Master clock** (MCLK):
    - Generated by DCO (but can also be fed by the crystal oscillator);
    - Activate and stable in less than 6 μsec;
    - Used by the CPU and high-speed peripherals.
  - **Subsystem main clock** (SMCLK):
    - Used as alternative clock source for peripherals.
  - **Auxiliary clock** (ACLK):
    - RTC self wake-up function from low power modes (32.768 kHz);
    - Always fed by the crystal oscillator.
  - Each clock can be internally divided by a factor of 1, 2, 4 or 8.

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System clocks (6/24)

- **Low/High frequency oscillator (LFXT1):**
  - Implemented in all MSP430 devices;
  - Used with either:
    - Low-frequency 32.768 kHz watch crystals (RTC);
    - Standard crystals, resonators, or external clock sources in range 450 kHz to 8 MHz (16 MHz in 2xx family).
  - The operating mode selection (one bit):
    - (=0) -> LF clock;
    - (=1) -> HF clock.
    - XTS: located at the BCSCTL1 register (2xx family);
    - XTS_FLL: located at the FLL_CTL0 register (4xx family).

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System clocks (7/24)

- **Second crystal oscillator (XT2):**
  - Sources of XT2CLK and its characteristics are identical to LFXT1 in HF mode (range 450 kHz to 8 MHz, or 16 MHz in the 2xx family);
  - Load capacitance for the high frequency crystal or resonator must be provided externally;
  - This oscillator can be disabled by the XT2OFF bit:
    - BCSCTL1 register in 2xx family;
    - FLL_CTL1 register in 4xx family (if XT2CLK is unused to source the MCLK and SMCLK clock signals).

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System clocks (8/24)

- **Digitally-controlled oscillator (DCO):**
  - Integrated ring oscillator with RC-type characteristics;
  - Provide a wide, software-controllable frequency range;
  - DCO frequency is synchronized to the FLL;
  - Frequency modulation method provided by FLL functionality:
    - **2xx family:**
      - Does not have full FLL functionality;
      - The DCO generates an internal signal (DCOCLK):
        - » Programmed internally or externally (DCOR bit);
        - » Controlled by a resistor connected to the R_{OSC} and V_{CC} pins.

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System clocks (9/24)

- **2xx family:**
  - The DCO control bits:
    - » RSELx: f_{DCO} range selection;
    - » DCOx: f_{DCO} defined by the RSEL bits. The step size is defined by the parameter SDCO;
    - » MODx: Modulation bits select how often f_{DCO}(RSEL, DCO+1) is used within the period of 32 DCOCLK cycles.
    - » The frequency f_{DCO}(RSEL, DCO) is used for the remaining cycles.
  - Specific frequency ranges and values vary by device:

$$f_{avg} = \frac{32 \times f_{DCO(RSEL,DCO)} \times f_{DCO(RSEL,DCO+1)}}{MOD \times f_{DCO(RSEL,DCO)} + (32 - MOD) \times f_{DCO(RSEL,DCO+1)}}$$

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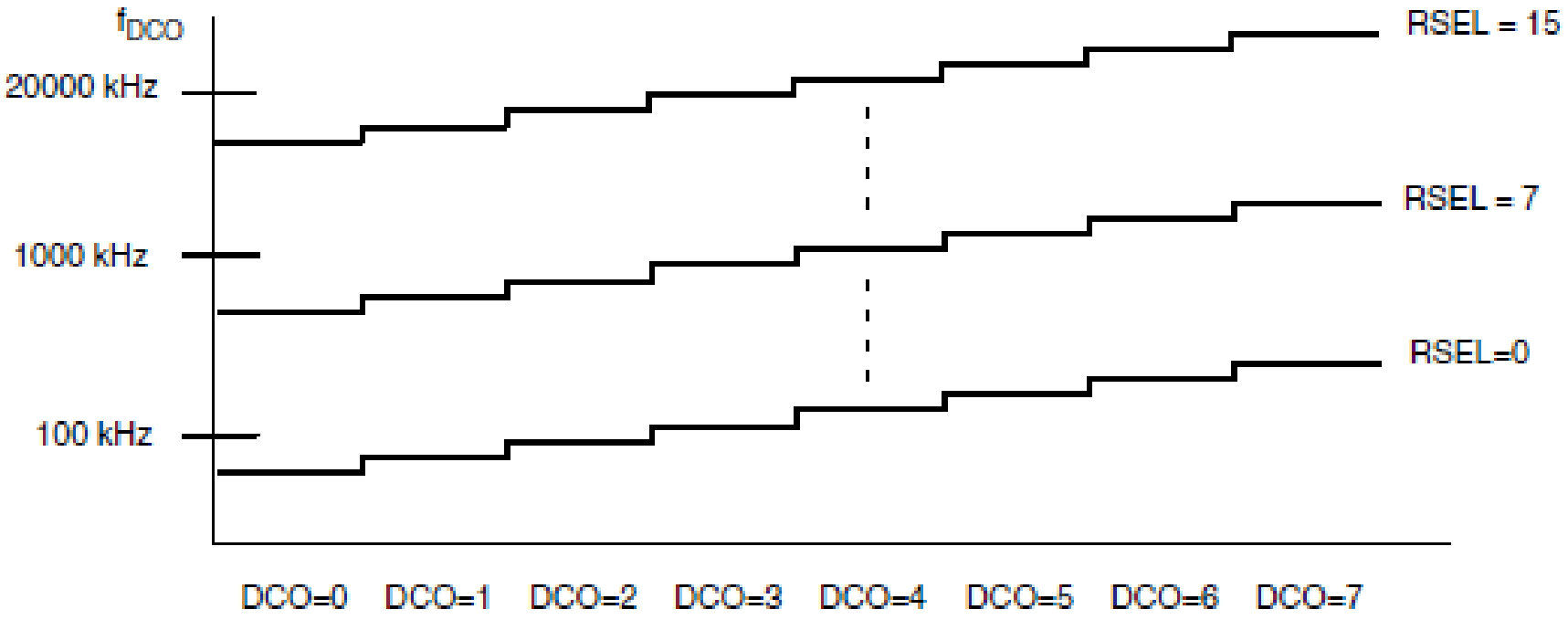

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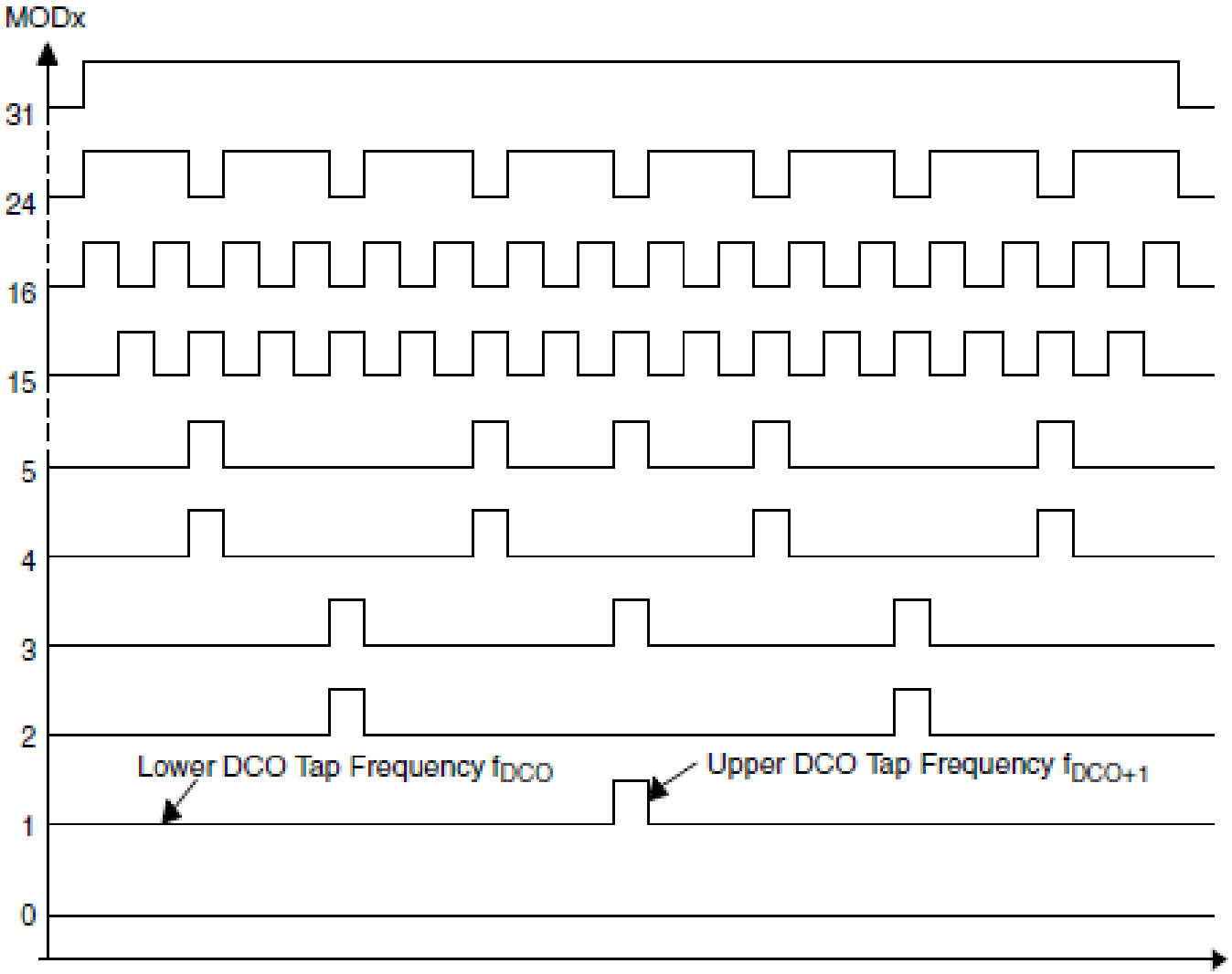

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System clocks (10/24)

- **2xx family:**
  - Basic Clock Module+ (BCM+) registers configuration:
    - » **DCOCTL: DCO Control Register**

7	6	5	4	3	2	1	0
DCOx			MODx				

Bit		Description
7-5	DCOx	Discrete DCO frequency selection step (depends on RSELx bits).
4-0	MODx	Modulator selection. These bits define how often the fDCO+1 frequency is used within a period of 32 DCOCLK cycles. During the remaining clock cycles (32−MOD) the fDCO frequency is used. Not useable when DCOx=7.

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System clocks (11/24)

- **2xx family:**
  - Basic Clock Module+ (BCM+) registers configuration:
    - » **BCSCTL1: Basic Clock System Control Reg. 1**

7	6	5	4	3	2	1	0
XT2OF	XTS	DIVAx		RSELx			

Bit		Description
7	XT2OF	XT2 oscillator fault: XT2OF = 0 ⇒ XT2 normal operation XT2OF = 1 ⇒ XT2 fault condition
6	XTS	LFXT1 oscillator operating mode: XTS = 0 ⇒ LF mode (low frequency) XTS = 1 ⇒ HF mode (high frequency)
5-4	DIVAx	ACLK frequency divider: DIVA1 DIVA0 = 0 0 ⇒ /1 DIVA1 DIVA0 = 0 1 ⇒ /2 DIVA1 DIVA0 = 1 0 ⇒ /4 DIVA1 DIVA0 = 1 1 ⇒ /8
3-0	RSELx	Range select. Sixteen different frequency ranges are available.

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System clocks (12/24)

- **2xx family:**
  - Basic Clock Module+ (BCM+) registers configuration:
    - » **BCSCTL2: Basic Clock System Control Reg. 2**

7	6	5	4	3	2	1	0
SELMx		DIVMx		SELS	DIVSx		DCOR

Bit		Description			
7-6	SELMx	MCLK source:	SELM1 SELM0 = 0 0 SELM1 SELM0 = 0 1 SELM1 SELM0 = 1 0 SELM1 SELM0 = 1 1	⇒ ⇒ ⇒ ⇒	DCO DCO XT2 LFXT1
5-4	DIVMx	MCLK frequency divider:	DIVM1 DIVM0 = 0 0 DIVM1 DIVM0 = 0 1 DIVM1 DIVM0 = 1 0 DIVM1 DIVM0 = 1 1	⇒ ⇒ ⇒ ⇒	/1 /2 /4 /8
3	SELS	SMCLK source:	SELS = 0 SELS = 1	⇒ ⇒	DCO XT2
2-1	DIVSx	SMCLK frequency divider:	DIVS1 DIVS0 = 0 0 DIVS1 DIVS0 = 0 1 DIVS1 DIVS0 = 1 0 DIVS1 DIVS0 = 1 1	⇒ ⇒ ⇒ ⇒	/1 /2 /4 /8
0	DCOR	DCO resistor selector	DCOR = 0 DCOR = 1	⇒ ⇒	Internal resistor External resistor

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System clocks (13/24)

- **2xx family:**
  - Basic Clock Module+ (BCM+) registers configuration:
    - » **BCSCTL3: Basic Clock System Control Reg. 3**

7	6	5	4	3	2	1	0
XT2Sx		LFXT1Sx		XCAPx		XT2OFF	LFXT1OF

Bit		Description				
7-6	XT2Sx	XT2 range select:	XT2S1 XT2S0 = 0 0	⇒	0.4 – 1 MHz	
			XT2S1 XT2S0 = 0 1	⇒	1 – 3 MHz	
			XT2S1 XT2S0 = 1 0	⇒	3 – 16 MHz	
			XT2S1 XT2S0 = 1 1	⇒	0.4 – 16-MHz (Digital external)	
5-4	LFXT1Sx	Low-frequency clock select and LFXT1 range select:		XTS=0:	XTS=1:	
			LFXT1S1 LFXT1S0 = 0 0 ⇒	32768 Hz	0.4 - 1-MHz	
			LFXT1S1 LFXT1S0 = 0 1 ⇒	Reserved	1 - 3-MHz	
			LFXT1S1 LFXT1S0 = 1 0 ⇒	VLOCLK	3 - 16-MHz	
			LFXT1S1 LFXT1S0 = 1 1 ⇒	External	0.4 - 16-MHz	
3-2	XCAPx	Oscillator capacitor selection:	XCAP1 XCAP0 = 0 0	⇒	~1 pF	
			XCAP1 XCAP0 = 0 1	⇒	~6 pF	
			XCAP1 XCAP0 = 1 0	⇒	~10 pF	
			XCAP1 XCAP0 = 1 1	⇒	~12.5 pF	
1	XT2OFF	XT2 oscillator fault:	XT2OFF = 0	⇒	No fault condition	
			XT2OFF = 1	⇒	Fault condition	
0	LFXT1OF	LFXT1OF oscillator fault:	LFXT1OF = 0	⇒	No fault condition	
			LFXT1OF = 1	⇒	Fault condition	

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System clocks (14/24)

- **4xx family:**
  - The DCO generates the signal: (f_{DCOCLK})=ACLK x D x (N+1).
  - The DCOPLUS bit sets the f_{DCOCLK} frequency to:
    - » f_{DCO};
    - » f_{DCO}/D: The FLLDx bits configure D=1, 2, 4 or 8.
  - By default, DCOPLUS = 0, D = 2 providing:
    - » f_{DCO}/2 on f_{DCOCLK};
    - » The multiplier (N+1) and D set the f_{DCOCLK}.
  - DCOPLUS = 0: $f_{DCOCLK} = (N + 1) \times f_{ACLK}$
  - DCOPLUS = 1: $f_{DCOCLK} = D \times (N + 1) \times f_{ACLK}$
  - f_{DCO} range selected by FNx bits (register SCFI0).

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System clocks (15/24)

- **Frequency Locked Loop (FLL) - 4xx family:**
  - Automatically modulates the DCO frequency;
  - Greater precision and control;
  - Mixes the programmed f_{DCO} with the next higher f_{DCO}.

  - **Operation:**
    - The DCO signal is divided by D and divided by N+1;
    - The signal obtained is continuously applied to the count down input of a 10-bit up/down counter (frequency integrator);
    - ACLK (LFXT1) is applied to the count up input of the counter;
    - The counter output is fed back to the DCO modulator, correcting and synchronizing the operating frequency;
    - The output of the frequency integrator can be read in SCFI1 and SCFI0 registers;
    - The count is adjusted by +1 each ACLK (xtal) period, by -1 each period of the divided DCO signal.

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System clocks (16/24)

- **Frequency Locked Loop (FLL) - 4xx family:**
  - 29 f_{DCO} taps are set by 5 of the integrator bits, SCFI1 bits 7 to 3 (28, 29, 30, and 31 are equivalent);
  - Each tap is approximately 10% higher than the previous;
  - The modulator mixes two adjacent DCO frequencies to produce fractional taps;
  - SCFI1 register bits 2 to 0 and SCFI0 register bits 1 to 0 are used for the digital modulator;
  - The method of FLL can be described as switching between the two most close neighbour frequencies to our frequency
    - To achieve the frequency requested as a time-weighted average of both frequencies.

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System clocks (17/24)

- **Frequency Locked Loop (FLL) - 4xx family:**
  - FLL+ clock module configuration:
    - **SCFQCTL: System Clock Control Register**

7	6	5	4	3	2	1	0
SCFQ_M	N						

Bit		Description		
7	SCFQ_M	Modulation control:		
		SCFQ_M = 0	⇒	FLL modulation enable
		SCFQ_M = 1	⇒	FLL modulation disable
6-0	N	DCO frequency multiplier factor:		
		DCOPLUS = 0	⇒	$f_{DCOCLK} = (N + 1) f_{crystal}$
		DCOPLUS = 1	⇒	$f_{DCOCLK} = D (N + 1) f_{crystal}$

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System clocks (18/24)

- **Frequency Locked Loop (FLL) - 4xx family:**
  - FLL+ clock module configuration:
    - **SCFI0: System Clock Frequency Integrator Reg. 0**

7	6	5	4	3	2	1	0
FLLDx		FN_x				MODx (LSBs)	

Bit		Description
7-6	FLLDx	FLL+ feedback loop f_{DCOCLK} divider: FLLD1 FLLD0 = 0 0 ⇒ /1 FLLD1 FLLD0 = 0 1 ⇒ /2 FLLD1 FLLD0 = 1 0 ⇒ /4 FLLD1 FLLD0 = 1 1 ⇒ /8
5-2	FN_x	f_{DCO} operating range: 0000 ⇒ 0.65 – 6.1 MHz 0001 ⇒ 1.3 – 12.1 MHz 001x ⇒ 2.0 – 17.9 MHz 01xx ⇒ 2.8 – 26.6 MHz 1xxx ⇒ 4.2 – 46.0 MHz
1-0	MODx	LSB modulator bits modified by the FLL+.

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System clocks (19/24)

- **Frequency Locked Loop (FLL) - 4xx family:**
  - FLL+ clock module configuration:
    - **SCFI1: System Clock Frequency Integrator Reg. 1**

7	6	5	4	3	2	1	0
DCOx					MODx (MSBs)		

Bit		Description
7-3	DCOx	DCO tap selection modified by the FLL+.
2-0	MODx	MSB modulator bits modified by the FLL+.

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System clocks (20/24)

❑ Frequency Locked Loop (FLL) - 4xx family:

- FLL+ clock module configuration:
  - **FLL_CTL0: FLL+ Control Register 0**

7	6	5	4	3	2	1	0
DCOPLUS	XTS_FLL	XCAPxPF		XT2OF	XT1OF	LFOF	DCOF

Bit		Description	
7	DCOPLUS	DCO output pre-divider:	DCOPLUS = 0 ⇒ Divider enable DCOPLUS = 1 ⇒ Divider disable
6	XTS_FLL	LFXT1 oscillator operating mode:	XTS_FLL = 0 ⇒ LF mode (low frequency) XTS_FLL = 1 ⇒ HF mode (high frequency)
5-4	XCAPxPF	LFXT1 oscillator load capacitance:	XCAP1PF XCAP0PF = 0 0 ⇒ ~ 1 pF XCAP1PF XCAP0PF = 0 1 ⇒ ~ 6 pF XCAP1PF XCAP0PF = 1 0 ⇒ ~ 8 pF XCAP1PF XCAP0PF = 1 1 ⇒ ~ 10 pF
3	XT2OF	XT2 oscillator fault:	XT2OF = 0 ⇒ XT2 normal operation XT2OF = 1 ⇒ XT2 fault condition
2	XT1OF	HF mode LFXT1 oscillator fault:	XT1OF = 0 ⇒ LFXT1 normal operation XT1OF = 1 ⇒ LFXT1 fault condition
1	LFOF	LF mode LFXT1 oscillator fault:	LFOF = 0 ⇒ LFXT1 normal operation LFOF = 1 ⇒ LFXT1 fault condition
0	DCOF	DCO oscillator fault:	DCOF = 0 ⇒ DCO normal operation DCOF = 1 ⇒ DCO fault condition

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System clocks (21/24)

❑ Frequency Locked Loop (FLL) - 4xx family:

- FLL+ clock module configuration:
  - **FLL_CTL1: FLL+ Control Register 0**

7	6	5	4	3	2	1	0
-	SMCLKOFF	XT2OFF	SELMx		SELS	FLL_DIVx	

Bit		Description				
6	SMCLKOFF	SMCLK disable:	SMCLKOFF = 0 SMCLKOFF = 1	⇒ ⇒	SMCLK enable SMCLK disable	
5	XT2OFF	XT2 disable:	XT2OFF = 0 XT2OFF = 1	⇒ ⇒	XT2 enable XT2 disable	
4-3	SELMx	MCLK source:	SELM1 SELM0 = 0 0 SELM1 SELM0 = 0 1 SELM1 SELM0 = 1 0 SELM1 SELM0 = 1 1	⇒ ⇒ ⇒ ⇒	DCO DCO XT2 LFXT1	
2	SELS	SMCLK source:	SELS = 0 SELS = 1	⇒ ⇒	DCO XT2	
1-0	FLL_DIVx	ACLK frequency divider:	FLL_DIV_0 = 0 0 FLL_DIV_1 = 0 1 FLL_DIV_2 = 1 0 FLL_DIV_3 = 1 1	⇒ ⇒ ⇒ ⇒	/1 /2 /4 /8	

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System clocks (22/24)

- **Internal clock signals:**
  - In 2xx family clock system = the basic clock module+:
    - Support for a 32768 Hz watch crystal oscillator;
    - Internal very-low-power low-frequency oscillator;
    - Internal digitally-controlled oscillator (DCO) stable <1 µs.
  - The BCM+ provides the following clock signals:
    - Auxiliary clock (ACLK), sourced either from:
      - » 32768 Hz watch crystal;
      - » Internal oscillator LFXT1CLK in LF mode with an internal load capacitance of 6 pF.
    - Main clock (MCLK), the system clock used by the CPU;
    - Sub-Main clock (SMCLK), the sub-system clock used by the peripheral modules.

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System clocks (23/24)

- **Internal clock signals:**
  - Both MCLK and SMCLK are sourced from DCOCLK at ~1.1 MHz but can be sourced up to 16 MHz;
  - 2xx DCO calibration data (in flash info memory segment A).

DCO frequency	Calibration register	Size	Address
1 MHz	CALBC1_1MHZ	Byte	010FFh
	CALBC0_1MHZ	Byte	010FEh
8 MHz	CALBC1_8MHZ	Byte	010FDh
	CALBC0_8MHZ	Byte	010FCh
12 MHz	CALBC1_12MHZ	Byte	010FBh
	CALBC0_12MHZ	Byte	010FAh
16 MHz	CALBC1_16MHZ	Byte	010F9h
	CALBC0_16MHZ	Byte	010F8h

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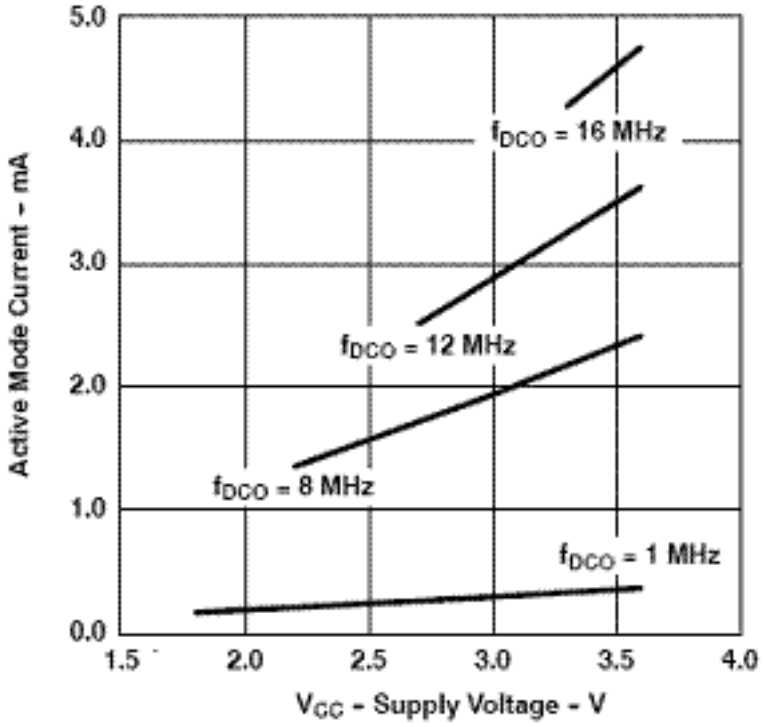
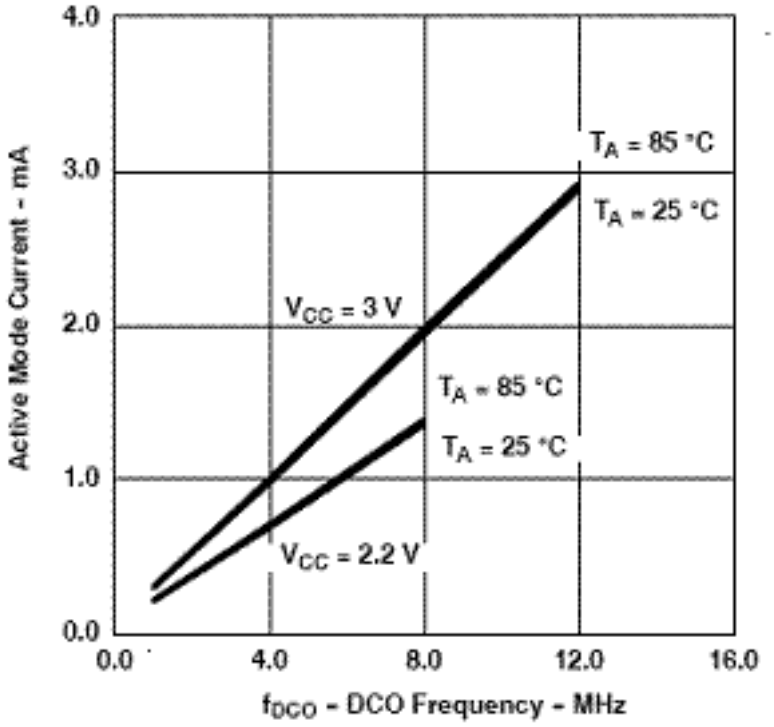
System clocks (24/24)

Internal clock signals:

- Electrical characteristics vary over the recommended supply voltage range of between 2.2 V and 3.6 V. Higher DCO frequencies require higher supply voltages.
- Typical characteristics in active mode supply current for the (2xx family):





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Interrupt management (1/8)

- **Interrupts:**
  - Are events applied to the application program that force a detour in program flow;
  - Cause CPU subprogram execution (ISR);
  - When Interrupt Service Routine (ISR) ends, the program flow returns to the previous state.
  - There are three classes of interrupts:
    - Reset;
    - Interrupts not maskable by GIE;
    - Interrupts maskable by GIE.

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Interrupt management (2/8)

- **The interrupts are used to:**
  - Allow a CPU fast response to a specific event;
  - Avoiding continuous polling for rare events;
  - Minimal disruption to the processing of other tasks.

- **In GIE-maskable interrupts, if both peripheral interrupt enable bit and GIE are set, when an interrupt is requested, it calls the ISR;**

- **The interrupt latency time:**
  - Δt between the event beginning and the ISR execution;
  - Interrupt latency time starts with acceptance of IR and counting until starting of first instruction of ISR.
    - Requiring 6 clock cycles

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Interrupt management (3/8)

- **During an interrupt event:**
  - PC of the next instruction and the SR are pushed onto the stack;
  - Afterwards, the SR is cleared with exception of SCG0, along with the appropriate interrupt, disabling interrupts (reset the GIE flag);
  - Other ISRs will not be called.

- **The RETI instruction at the end of the ISR will return to the original program flow, automatically popping the SR and PC;**

- **Ensure that:**
  - The ISR processing time is less than the interrupt's request time interval;
  - To avoid stack overflow -> application program collapse.

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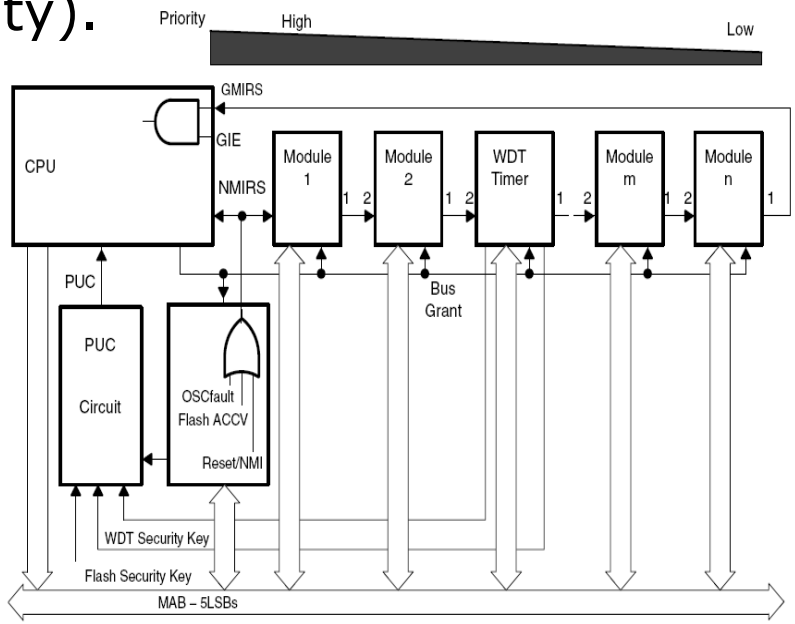
Interrupt management (4/8)

- **Types of interrupts (internal and external):**
  - Reset;
  - Interrupts not maskable by GIE: (non)-maskable interrupts (NMI);
  - Interrupts maskable by GIE.

  - Interrupts priority (The nearer a module is to the CPU/NMIRS, the higher the priority).



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Interrupt management (5/8)

Types of interrupts (internal and external):

- Main differences between non-maskable and maskable interrupts:
  - Non-maskable interrupts cannot be disabled by the GIE bit of the SR. Used for high priority events e.g. emergency shutdown;
  - Maskable interrupts are recognized by the CPU's interrupt control, so the GIE bit must be set.
    - Can be switched off by software.
- The system reset interrupts (Oscillator/Flash and the Hard Reset) are treated as highest priority non-maskable interrupts, with their own interrupt vectors.

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Interrupt management (6/8)

- **Types of interrupts (internal and external):**
  - **Non Maskable Interrupts:**
    - Not masked by GIE;
    - Enabled by individual interrupt enable bits;
    - Depend on the event source:
      - **NMIIE**: Non-Maskable Interrupts Interrupt Enable:
        - » RST/NMI is configured in NMI mode;
        - » A signal edge selected by the WDTNMIES bit generates an NMI;
        - » The RST/NMI flag NMIIFG is also set.
      - **ACCVIE**: ACCess Violation to the flash memory Interrupt Enable:
        - » The flash ACCVIFG flag is set.
      - **OFIE**: Oscillator Fault Interrupt Enable:
        - » This signal can be triggered by a PUC signal.

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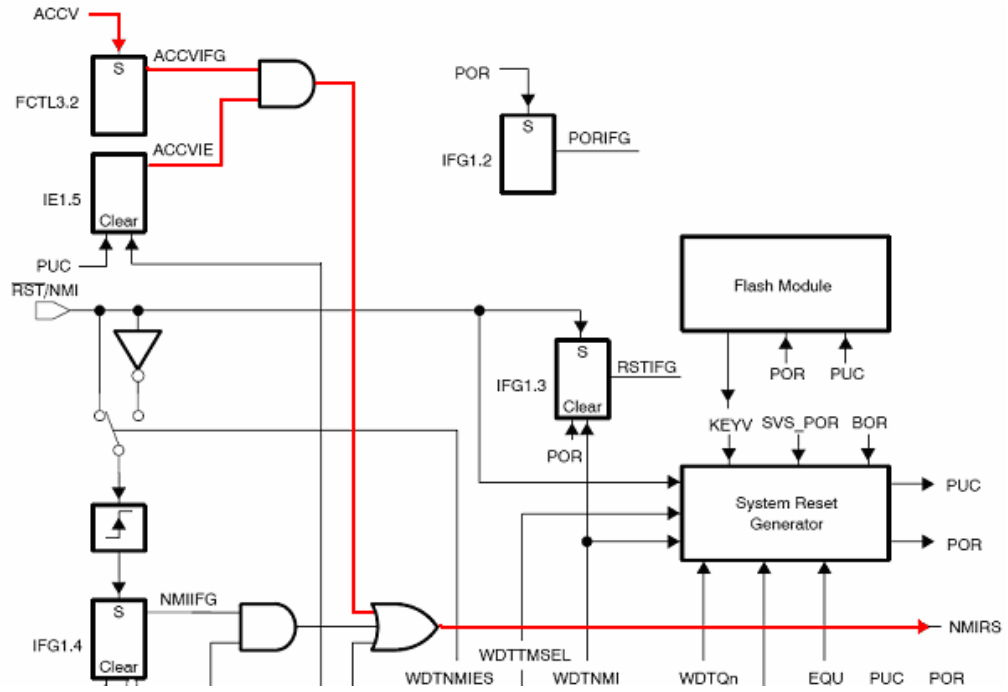
Interrupt management (7/8)

- **Types of interrupts (internal and external):**
  - **Non Maskable Interrupts:**
    - Example: ACCVIE (2xx family).

ACCV=1 → ACCVIFG=1

ACCVIFG=1 and ACCVIE=1 (set by software) → NMIRS=1



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Interrupt management (8/8)

- **Types of interrupts (internal and external):**
  - **(by GIE) Maskable Interrupts:**
    - Peripherals with interrupt capability or the watchdog timer overflow in interval timer mode;
    - Individual enable/disable flag, located in peripheral registers or in the individual module;
    - Can be disabled by resetting the GIE bit in SR, either by software or by hardware/interrupt.

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Watchdog timer (WDT and WDT+) (1/4)

- **The 16-bit WDT module can be used in:**
  - **Supervision mode:**
    - Ensure the correct working of the software application;
    - Perform a PUC;
    - Generate an interrupt request after the counter overflows.
      - When the software to hang or enter an infinite loop
  - **Interval timer:**
    - Independent interval timer to perform a “standard” interrupt upon counter overflow periodically;
    - Upper counter (WDTCNT) is not directly accessible by software;
    - Control and the interval time selecting WDTCTL register;
    - WDTCNT: clock signal ACLK or SMCLK (WDTSSEL bit).

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Watchdog timer (WDT and WDT+) (2/4)

- **The WDT control is performed through the:**
  - **WDTCTL, Watchdog Timer Control Register, WDTCTL**

    - Eight MSBs (WDTPW): Password function, read as 0x69h, write as 0x5Ah unless the user want to force a PUC from software.

15	8
Read with the value 0x69h,	WDTPW write with the value 0x5Ah

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Watchdog timer (WDT and WDT+) (3/4)

- **The WDT control is performed through the:**
  - **WDTCTL, Watchdog Timer Control Register, WDTCTL**

    - Eight LSBs: WDT configuration

7	6	5	4	3	2	1	0
WDTHOLD	WDTNMIES	WDTNMI	WDTTMSEL	WDTCNTCL	WDTSSEL	WDTIS1	WDTIS0

Bit		Description	
7	WDTHOLD	WDT hold when WDTHOLD = 1. Useful for energy economy.	
6	WDTNMIES	Select the NMI interrupt edge when WDTNMI = 1	WDTNMIES = 0 ⇒ NMI on rising edge WDTNMIES = 1 ⇒ NMI on falling edge
5	WDTNMI	Select the RST/NMI pin function	WDTNMI = 0 ⇒ Reset function WDTNMI = 1 ⇒ NMI function
4	WDTTMSEL	Select the WDT mode:	WDTTMSEL = 0 ⇒ Supervision mode WDTTMSEL = 1 ⇒ Interval timer mode
3	WDTCNTCL	WDT counter clear:	WDTCNTCL = 0 ⇒ No action WDTCNTCL = 1 ⇒ Counter initialization at 0x0000h
2	WDTSSEL	Select the WDT clock signal:	WDTSSEL = 0 ⇒ SMCLK WDTSSEL = 1 ⇒ ACLK
1-0	WDTISx	Select the WDT timer interval:	WDTIS1 WDTIS0 = 0 0 ⇒ Clock signal / 32768 WDTIS1 WDTIS0 = 0 1 ⇒ Clock signal / 8192 WDTIS1 WDTIS0 = 1 0 ⇒ Clock signal / 512 WDTIS1 WDTIS0 = 1 1 ⇒ Clock signal / 64

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Watchdog timer (WDT and WDT+) (4/4)

- **The WDT uses two bits in the Special Function Registers (SFRs) for interrupt control:**
  - **WDTIE**: WDT interrupt enable (IE1.0):
    - Enables the WDTIFG interrupt for interval timer mode when WDTIE=1.
  - **WDTIFG**: WDT interrupt flag (IFG1.0):
    - *Supervision mode*:
      - » WDTIFG sources a reset vector interrupt.
      - » If WDTIFG=1, the WDT initiates the reset condition (detectable reset source).
    - *Interval mode*:
      - » WDTIFG set after the selected time interval and requests a WDT interval timer interrupt;
      - » If WDTIE and GIE bits set;
      - » WDTIFG reset automatically (also can be reset by software).

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Supervisory Voltage System (SVS) (1/2)

- **Used to monitor:**
  - AV_{CC} supply voltage;
  - External voltage (located at the SVSIN input).
    - The core of this module is an analogue comparator
- **When AV_{CC} or SVSIN drops below selected threshold:**
  - Sets a flag generating an interrupt;
  - Generates a system reset (POR).
- **Is disabled after a BOR to conserve current consumption;**
- **SVS features:**
  - Output of SVS comparator accessible by software;
  - Low-voltage condition latched (accessible by software);
  - 14 selectable threshold levels;
  - External channel to monitor external voltage.

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Supervisory Voltage System (SVS) (2/2)

- **SVS control performed by:**
  - **SVSCTL, SVS Control Register**

7	6	5	4	3	2	1	0
VLDx				PORON	SVSON	SVSOP	SVSFG

Bit		Description			
7-4	VLDx	Voltage level detect.	VLD3 VLD2 VLD1 VLD0 = 0000	⇒	SVS is off
			VLD3 VLD2 VLD1 VLD0 = 0001	⇒	1.9 V
			VLD3 VLD2 VLD1 VLD0 = 0010	⇒	2.1 V
					.
					.
					.
			VLD3 VLD2 VLD1 VLD0 = 1101	⇒	3.5 V
			VLD3 VLD2 VLD1 VLD0 = 1110	⇒	3.7 V
			VLD3 VLD2 VLD1 VLD0 = 1111	⇒	SVSIN to 1.25V
3	PORON	When PORON = 1 enables the SVSFG flag to cause a POR device reset			
2	SVSON	This bit reflects the status of SVS operation, being set (SVSON=1) when the SVS is on			
1	SVSOP	This bit reflects the output value of the SVS comparator: SVSOP = 0 ⇒ SVS comparator output is low SVSOP = 1 ⇒ SVS comparator output is high			
0	SVSFG	When SVSFG=1 a low voltage condition occurs			

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